UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/680,509	10/07/2003	Kuang Chien Hsieh	10322/57	5043

7590 08/23/2006

Brinks Hofer Gilson & Lione
P.O. Box 10395
Chicago, IL 60610

EXAMINER	
TRINH, HOA B	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 08/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/680,509	HSIEH ET AL.	
	Examiner	Art Unit	
	Vikki H. Trinh	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *30-53,72-82 and 101-131* is/are pending in the application.

4a) Of the above claim(s) *72-77 and 81* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *30-53,78-80,82 and 101-131* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/18/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 06/26/2006 has been entered.

Acknowledgement

The amendment filed on 06/26/2006 has been considered. Claims 30-53, 72-82, 101-131 are pending. Claims 1-29, 54-71, 83-100 have been canceled. Claims 72-77 and 81 have been withdrawn.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 30-53, 78-80, 101-110, 112-119 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (hereinafter Lee, EP 1246238 A2, applicant cited reference). in view of Malik et al. (6,881,644) (hereinafter Malik).

Lee discloses a method of bonding two structures (figs. 4a-4b) together, the method comprising depositing low temperature grown semiconductor bonding layers 13 on placing the bonding Layers 13 (fig. 4b) in contact with each other; applying pressure to the combined structure (fig. 4b), and first and second structures A,B (fig. 4b) to form a combined structure (fig. 4b), annealing the combined structure under conditions sufficient for the bonding Layers 13 to bond the first and second structures together (figs. 4a-4b). (see also page 5, line 50, page 6, lines 53, 56, 57, 59). Note that layer 13 can be selected with Ga-rich material (see page 5)

However, Lee does not explicitly teach that at least one of the bonding layers comprises an amorphous material, and the step of annealing of the combined structure occurs at a temperature of between about 300°C and 700°C and for a time sufficient for the bonding layers which crystallizes at least a portion of the amorphous material to a polycrystalline material.

Malik discloses an analogous method and device having the steps of bonding two structures (fig. 3D) together, the method comprising depositing low temperature grown semiconductor bonding layers on placing the bonding Layers 54, 52 (fig. 3D) in contact with each other; applying pressure (col. 11, lines 60-65) to the combined structure (fig. 3D), and first and second structures (figs. 2E, 3B, 3D)to form a combined structure (fig. 3D), annealing (col. 7, lines 55-65) the combined structure under conditions sufficient for the bonding Layers 54, 52 to bond the first and second structures together (figs. 2E, 3B, 3D). As to claim 33, the bonding Layer comprises at least one of amorphous and polycrystalline (Ga,As or P) (col. Col. 8, lines 1-10) and the annealing of the combined structure occurs at a temperature of between about 300C and 700C and for a time sufficient for the bonding Layers to form a (Ga,As) material that is substantially entirely polycrystalline (col. 12, lines 40-50). Also, by annealing of the combined structure occurred under conditions sufficient for the bonding layers crystallizes into a polycrystalline material (see abstract).

Therefore, as to claims 30, 33-34, 101-102, 105-107,116, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Lee with the annealing step as taught by Malik so as to provide the bonding the of the structure with crystallized material (Malik, col. 12, lines 40-50).

As to claims 31, 103, 121, 127, Lee discloses the method of claim 30, further comprising applying the pressure substantially uniformly to the combined structure A, B (fig. 4b) during annealing (page 5, line 50, page 6, lines 53, 56, 57, 59).

As to claims 32,104, Lee discloses the method of claim 30, wherein the annealing of the

combined structure A,B (fig. 4b) occurs under conditions sufficient for the bonding layers to form a polycrystalline material (page 5, line 50, page 6, lines 53, 56, 57, 59, and abstract).

As to claim 35, 120, 122, 123, 126, 129,128, Malik teaches the bonding Layer (fig. 3D) comprises at least one of amorphous and polycrystalline (Ga,N) and the annealing of the combined structure occurs at a temperature of between about 700C and 900C and for a time sufficient for the bonding layers to form a (Ga,N) material that is substantially entirely polycrystalline (col. 12, lines 1-15).

As to claim 43, 111, 124, 125, 130-131, Malik's step of deposition deposits at least one of low temperature grown (Ga,As), (Ga,P) and (Ga,N) on at least one of the first and second structures. (col. 14, lines 53-67)

As to claims 36, 118, Lee discloses the bonding layers 13 (fig. 4b) are placed in contact with each other without regard for a relative angular orientation of the first and second structures (fig. 4b) to each other.

As to claims 37, 108, Lee discloses at least one of the first and second structures comprises a non-semiconductor substrate (fig. 4a-4b).

As to claim 38, Lee discloses the method further comprising fabricating at least one of an electronic and optoelectronic device from the combined structure (fig. 4b)

As to claims 39, 109, Lee discloses the annealing of the combined structure occurs under conditions that are not damaging to the first and second structures but are sufficient to form bonds that are strong enough to survive subsequent processing at temperatures higher than that used during the bonding (see abstract).

As to claims 40, 110, Lee discloses a bonding interface produced by the annealing is substantially optically transparent to light emitted by the combined structure (see abstract).

As to claims 41, 112, Lee discloses a bonding interface produced by the annealing is strong enough to be substantially unaffected by processing of the combined structure (see abstract).

As to claim 42, Lee discloses the deposition deposits between about 3 nm and about 600 nm of material on each of the first and second structures (fig. 4a-4b).

As to claims 44, 113, Lee discloses the method includes selecting a composition of the bonding layer such that an amorphous layer is deposited on at least one of the first and second structures A,B (fig. 4b). (see abstract).

As to claims 45, 114, Lee discloses the annealing of the combined structure occurs under conditions sufficient for the bonding layers to form a polycrystalline material from the amorphous layer see abstract.

As to claims 46, Lee discloses the method includes selecting a composition of the bonding Layer such that a polycrystalline semiconductor Layer is deposited on at least one of the first and second structures A,B (fig. 4b) (see abstract).

As to claims 47, 115, Lee discloses the annealing of the combined structure occurs under conditions sufficient for the bonding Layers to recrystallize into a polycrystalline material (see abstract).

As to claim 48, 116, the annealing occurs at temperatures of at most about 800C (col. 12, lines 45-50).

As to claim 49, Lee discloses the bonding layer comprises a compound semiconductor (page 5, line 50).

As to claim 50, the method includes doping the bonding layer with Si (col. 8, lines 1-15).

As to claim 101, Ga-rich low temperature grown semiconductor bonding Layers are deposited (col. 8, lines 1-10).

As to claims 51, 117, Lee discloses the step of doping the bonding layer with a dopant that helps to control morphology of the compound semiconductor (see abstract).

As to claim 52, Lee discloses the structures A, B (fig. 4a-4b) are separate structures and the bonding layers 13 place in contact and the combined structure is annealed.

As to claims 53, 119, Lee discloses the bonding Layer 13is deposited by molecular beam epitaxy (MBE) at a temperature of at most about 100C (page 5, line 50).

As to claim 78, Lee discloses at least one of the first and second structures A,B comprises a semi-insulating substrate (fig. 4a-4b).

As to claim 79, Lee discloses the structures include an insulator (fig. 4a-4b).

As to claim 80, Lee discloses the structures are a "pseudomorphic" structure (fig. 4a-4b).

As to claim 82, Lee discloses the bonding layer 13 is devoid of polymers, metal, and ceramics (see abstract).

Response to Arguments

5. Applicant's arguments with respect to the pending claims have been considered but they are not persuasive.

The rejection of claims 30-32, 36-42, 44-47, 49, 51-53, 78-80 101-104, 108-110, 112-114, 117-119 under 35 USC 102 is moot in view of the new rejection.

In the remarks, applicants argue the rejection of the amended claims 33-35, 43, 48, 50, 101, 105-107, 116, that the amended claims overcome the art rejection. The examiner disagrees. The amended claims are still too broad to overcome the art rejection. As stated in the above rejection, Lee discloses all of the steps, except that Lee does not explicitly teach that at least one of the bonding layers comprises an amorphous material, and the step of annealing of the combined structure occurs at a temperature of between about 300°C and 700°C and for a time sufficient for the bonding layers which crystallizes at least a portion of the amorphous material to a polycrystalline material. Malik discloses an analogous method and device having the steps of bonding two structures (fig. 3D) together, the method comprising depositing low temperature grown semiconductor bonding layers on placing the bonding layers 54, 52 (fig. 3D) in contact with each other; applying pressure (col. 11, lines 60-65) to the combined structure (fig. 3D), and first and second structures (figs. 2E, 3B, 3D)to form a combined structure (fig. 3D), annealing (col. 7, lines 55-65) the combined structure under conditions sufficient for the bonding Layers 54, 52 to bond the first and second structures together (figs. 2E, 3B, 3D). As to claim 33, the bonding layer comprises at least one of amorphous and polycrystalline (Ga,As or P) (col. Col. 8, lines 1-10) and the annealing of the combined structure occurs at a temperature of between about 300C and 700C and for a time sufficient for the bonding layers to form a (Ga,As) material that is substantially entirely polycrystalline (col. 12, lines 40-50). Also, by annealing of the combined structure occurred under conditions sufficient for the bonding layers crystallizes into a polycrystalline material (see abstract). (Note that the cited references should be read as a whole, not in p[art). Thus, Malik cures the deficiency of Lee.

For the fore going reasons, the rejection is maintained.

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Vikki Trinh whose telephone number is (571) 272-1719. The Examiner can normally be reached from Monday-Friday, 9:00 AM - 5:30 PM Eastern Time. If attempts to reach the examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Wael Fahmy, can be reached at (571) 272-1705. The office fax number is 703-872-9306.

Any request for information regarding to the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Also, status information for published applications may be obtained from either Private PAIR or Public Pair. In addition, status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. If you have questions pertaining to the Private PAIR system, please contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site (www.uspto.gov), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at http://www.uspto.gov/ebc/index.html or 1-866-217-9197 for information on this policy. Requests

to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

Vikki Trinh,
Patent Examiner
AU 2814

HOWARD WEISS
PRIMARY EXAMINER